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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,432	12/15/2000	Jun Souk Joung	HI-023	8762

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EXAMINER	
DIVECHA, KAMAL B	
ART UNIT	PAPER NUMBER
2151	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/736,432	JOUNG, JUN SOUK	
	Examiner	Art Unit	
	KAMAL B. DIVECHA	2151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20061213*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

Claims 1-5, 7-11, 13-20, 22-27 are pending in this application.

Claims 6, 12 and 21 are cancelled in this application.

In view of the telephone conversation on December 13, 2006, Examiner hereby withdraws the office action (final rejection) issued on December 1, 2006 (See Interview Summary).

A new office action (i.e. non final rejection) has been issued accordingly.

Applicant's arguments with respect to claims 1-5, 7-11, 13-20, 22-27 have been considered but are moot in view of the new ground(s) of rejection, as necessitated by the substantial amendments through the incorporation of the limitation of claim 6 into the independent claim 1 as well as cancellation of claim 6, 12 and 21.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-5, 7-11, 13-20, 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoon (US 5,978,589) in view of Hirasawa et al. (hereinafter Hirasawa, US 5,655,079), and further in view of Kurdzo et al. (hereinafter Kurdzo, US 5,469,434).

As per claim 1, Yoon teaches a method for down-loading data from an upper processor to a plurality of lower processors "middle processors" of a mobile communications switching

system "base station system" in a process of resetting (processor being initialized after power source is applied) the processors, the method comprising (Col 2, lines 30-45, Fig 2):

requesting an information download from the lower processors to the upper processor (Col 2, lines 40-50);

accessing a memory of the upper processor containing the requested information download (Col 2, lines 40-50);

determining whether the accessed information has an error (Yoon teaches the need to reduce the time taken to download configuration files to multiple processors in a mobile system (Col 1, lines 35-45). Yoon further teaches the need to have a completion signal to insure that the files are ready to be deployed (Col 2, lines 45-55). To be complete, it is important that the file in question is error free for the operation to be successful);

transferring the information from the upper processor to the lower processors (Col 2, lines 45-55, fig. 3 item #100, 104, 106);

However, Yoon does not teach the process of grouping the lower processors with a representative address by creating the accessed information in an information processing code (IPC) format supported by error checking; and wherein group information is used to determine the group representative address, and wherein the group information comprises a node address, a processor ID, a cinu address and a slot address.

Hirasawa, from the same field of endeavor teaches a solution on reducing the time to download to multiple computers (each computer represent a processor) while providing means for error checking (Col 10, lines 55-65). Hirasawa teaches the process of creating the

accessed information in an information processing code IPC format (Fig 7) (Col 4, lines 50-65); determining whether the accessed information has an error (Col 10, lines 55-65); and transferring the IPC format information from the upper processor to the lower by using the group representative address, the transferred IPC format information including the accessed information and the group representative address, wherein group information is used to determine the group representative address, and wherein the group information comprises a node address, physical addresses of processors, and cinu address (i.e. a network ID) (Col 7, lines 35-50) (Col 16, lines 10-20, col. 17 L19-50: please note that an IP address has both the node address and network ID).

Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Yoon in view of Hirasawa in order to transfer the information in an IPC format utilizing the group address.

One of ordinary skilled in the art would have been motivated because Hirasawa method provided an improvement approach to the downloading of code, which allowed one format to be used for group and individual download which reduces network traffic (Col 1, lines 35-45) (Col 2, lines 30-35). By allowing group downloading, the time taken to configure all the processors is less.

However, Yoon in view of Hirasawa does not disclose the process wherein the group information comprises processor ID (BHIU address), and a slot address (SA).

Kurdzo, from the same field of endeavor discloses the process of addressing the group of processors by using the slot number, processors type and id as disclosed by soft address, and further teaches the process wherein each processor in the system to be addressed as part

of the subgroup or collection (col. 8 L22 to col. 9 L44).

Therefore It would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Yoon in view of Hirasawa in view of Kurdzo in order to use the slot number, processor id or configuration, in addressing the group address.

One of ordinary skilled in the art would have been motivated because this level of addressing would have allowed any collection of processors to be accessed simultaneously (Kurdzo, col. 8 L29-55, col. 9 L1-9).

As per claim 2, Yoon combined with Hirasawa, teaches about a method of claim 1, wherein the resetting of the processors includes an initial loading and a re-loading (Yoon Col 2, lines 30-45).

As per claim 3, Yoon combined with Hirasawa, teaches about a method of claim 1, wherein the group representative address includes all the lower processors (Yoon Col 2, lines 30-45) (Hirasawa Col 4, lines 20-35).

As per claim 4, Yoon combined with Hirasawa, teaches about a method of claim 1, wherein the grouping the lower processors comprises grouping the plurality of lower processors using the group representative address (Yoon Col 2, lines 30-45) (Hirasawa Col 4, lines 20-35).

As per claim 5, Yoon combined with Hirasawa, teaches about a method of claim 1, wherein the grouping the lower processors comprises grouping at least one additional lower processor "lower processor" (Yoon Col 2, lines 30-45) (Hirasawa Col 4, lines 20-35).

As per claim 7, Yoon in view of Hirasawa does not disclose the process wherein the group representative address, is set by using the network id (CA) and slot address, among the group information.

However, Yoon, Hirasawa does teach the process of generating a group address by using the node address and the network Id (Hirasawa, Col 7, lines 35-50, Col 16, lines 10-20, col. 17 L19-50, fig. 1, fig. 5b: also note that, processor id, slot address, etc., are all well known identifiers in the relevant art). Kurdzo further teaches the process of using the slot number and the aggregates in addressing the group of processors (Kurdzo, col. 8 L22 to col. 9 L44).

Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Yoon and Hirasawa in view of Kurdzo in order to group the processors, by setting the group address comprising the network id and the slot address.

One of ordinary skilled in the art would have been motivated for the same reasons as set forth in claim 1.

As per claim 8, Yoon in view of Hirasawa and Kurdzo discloses the process wherein grouping of the group representative address is responsive to one of only the CA (network ID) among the group information, only the SA (slot address) among the group information and both the CA and SA among the group information (fig. 1, fig 5b, Col 7, lines 35-50, Col 16, lines 10-20: please note that an IP address has both the node address and network ID).

As per claim 9, Yoon in view of Hirasawa and Kurdzo discloses the process wherein the IPC format information is concurrently transferred to all the lower processors using the group representative address (Hirasawa, Col 7, lines 35-50, Col 16, lines 10-20).

As per claim 25, Yoon combined with Hirasawa, teaches about a method wherein group representative address comprises an address of at least two of the lower processor (Hirasawa Col 4, lines 20-30) (Hirasawa Col 16, lines 10-20) (Covered in claim 1).

As per claims 10, 11, 13-20, 22-24 and 26-27, they do not teach or further define over the limitations in claims 1-5, 7-9 and 25. Therefore claims 10, 11, 13-20, 22-24 and 26-27 are rejected for the same reasons a set forth in claims 1-5, 7-9 and 25.

Additional References

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Yamazaki, US 5,923,855 Multi-Processor system and method for synchronizing among the processors.

b. Dewa et al., US 5,634,071: Synchronous Processing Method and Apparatus for a plurality of processors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAMAL B. DIVECHA whose telephone number is 571-272-5863. The examiner can normally be reached on Increased Flex Work Schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarni Maung can be reached on 571-272-3939. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kamal Divecha
Art Unit 2151
December 13, 2006.

ZARNI MAUNG
SUPERVISORY PATENT EXAMINER